

# EXPLORING ALGEBRAIC METHODS FOR CIRCUIT VERIFICATION

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TU Wien

Vienna, Austria

Dagstuhl Seminar

**Theory and Practice of SAT and Combinatorial Solving**

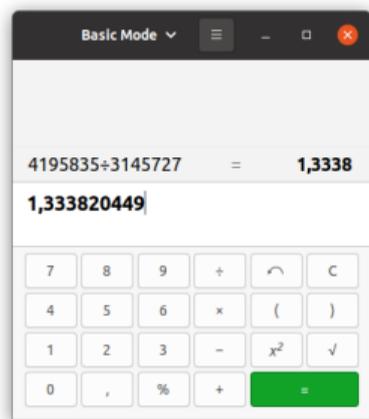
Dagstuhl, Germany

October 9-14, 2022

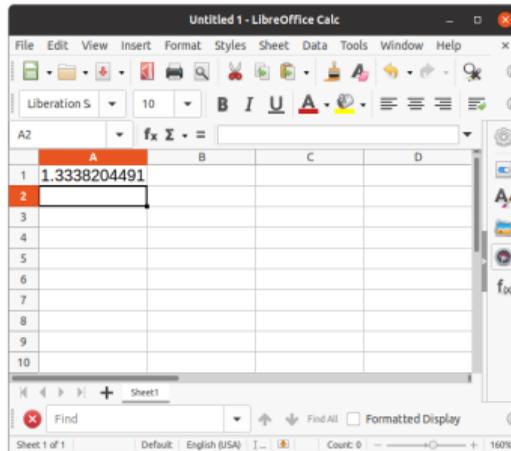
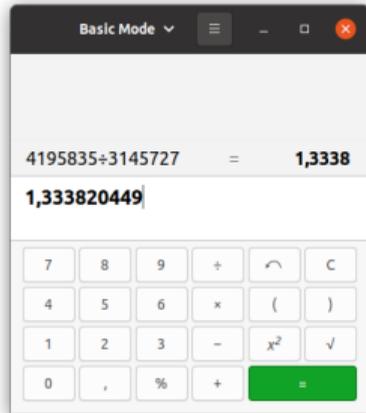


$$4\,195\,835 \div 3\,145\,727 = ?$$

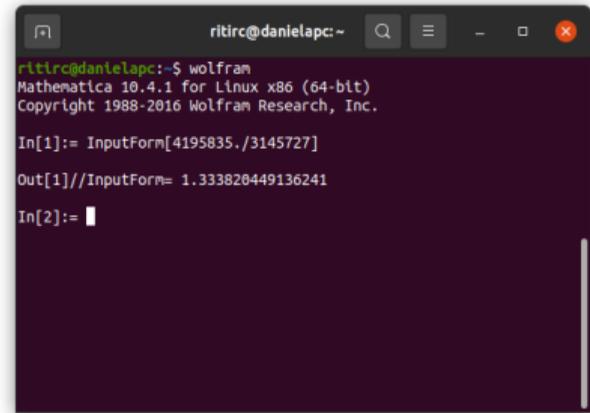
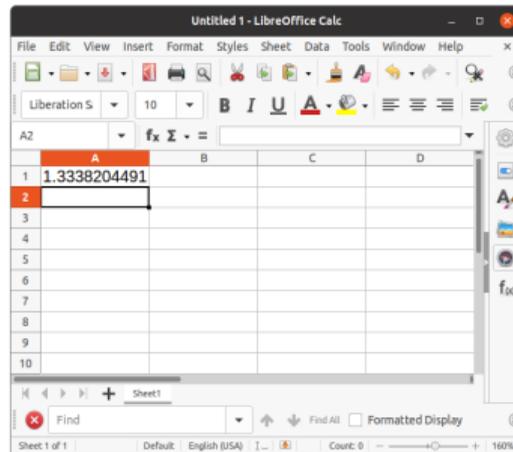
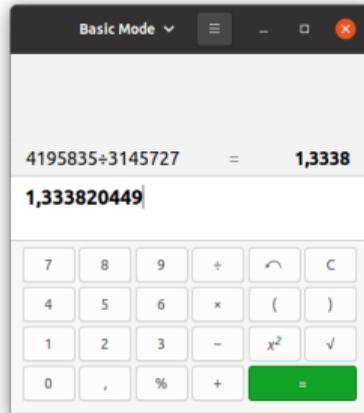
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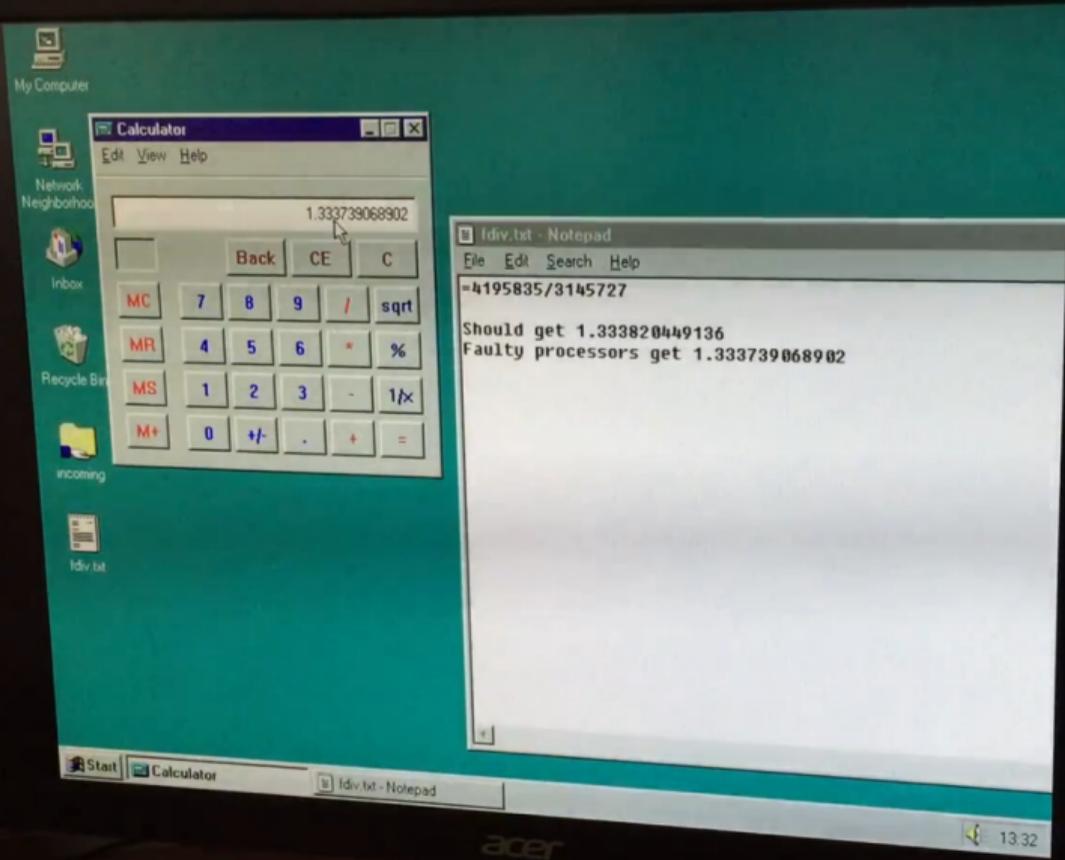


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# Intel Pentium FDIV bug 1994



<http://neology.com.au/portfolios/a80502-90-sx923/>

- Affected floating point unit (FPU) in early Intel processors.
- Processor might return incorrect result for division.
- Cost in 1994: 500 million dollars.

Even more than 25 years later, verification of arithmetic circuits is considered to be hard. Especially proving the correctness of gate-level integer multiplier circuits is a challenge.

# Multiplication

$$\begin{array}{r} 11 \cdot 11 \\ \hline \end{array}$$

$$3 \cdot 3 = 9$$

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$$\begin{array}{r} 11 \cdot 11 \\ \hline 11 \\ 110 \\ \hline 121 \end{array}$$

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## Multiplication

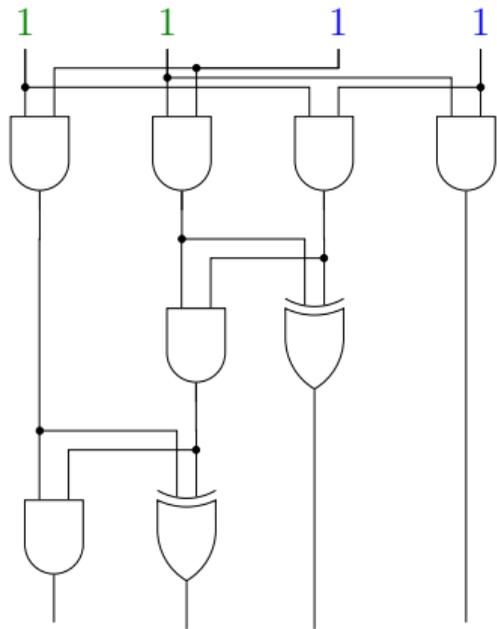
$$\begin{array}{r} 11 \cdot 11 \\ \hline \phantom{11} 11 \\ \phantom{1} 110 \\ \hline 1001 \end{array}$$

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# Multiplication

## AND-Gate



$$f \wedge g = y$$

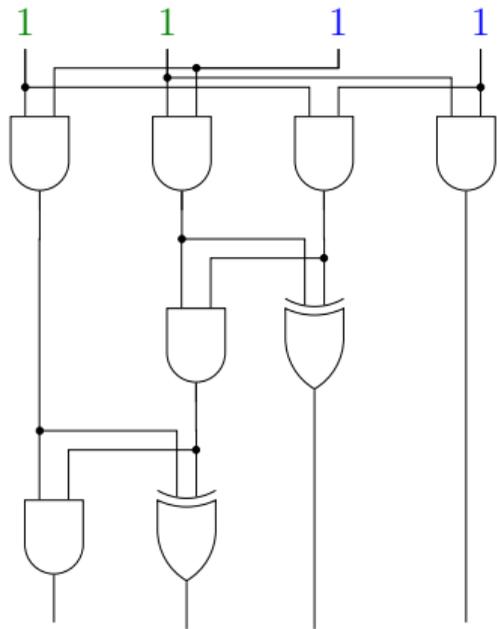
$f$	$g$	$y$
0	0	0
0	1	0
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1	1	1

## XOR-Gate



$$f \oplus g = y$$

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# Multiplication

## AND-Gate



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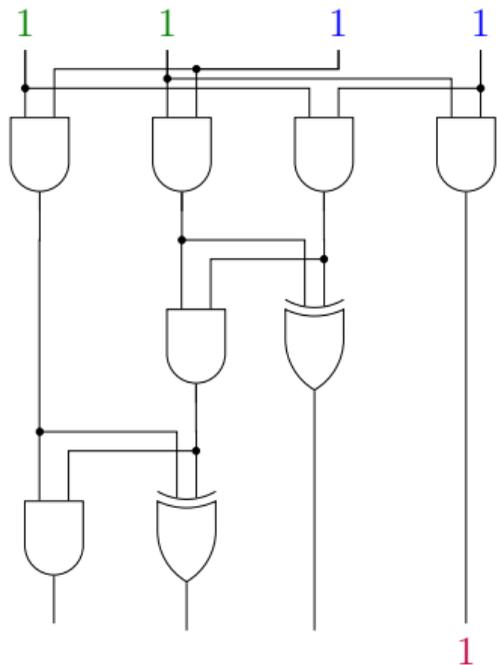
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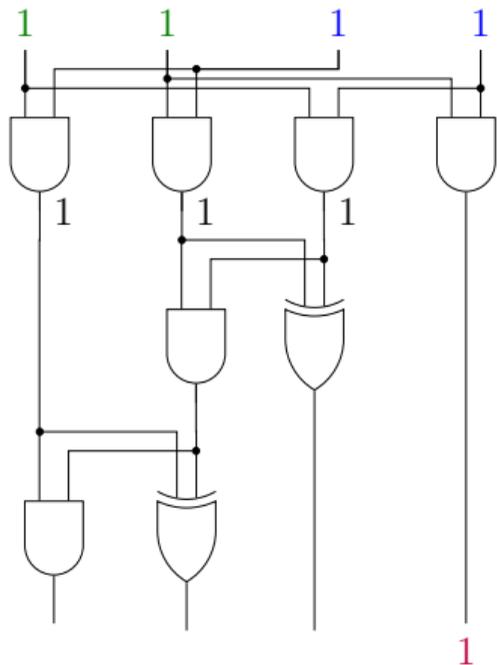
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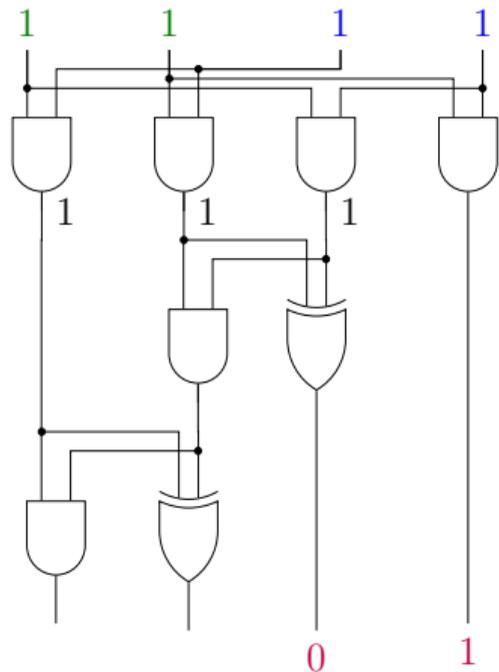
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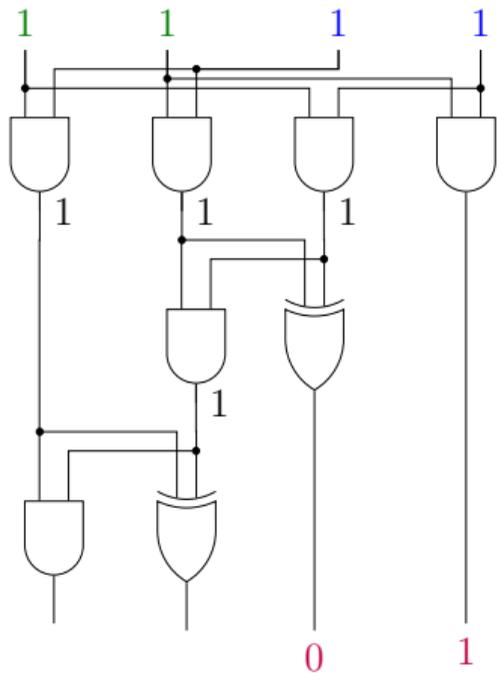
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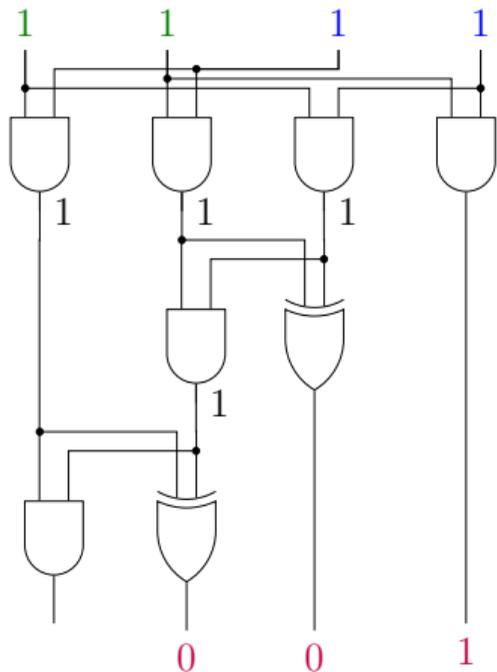
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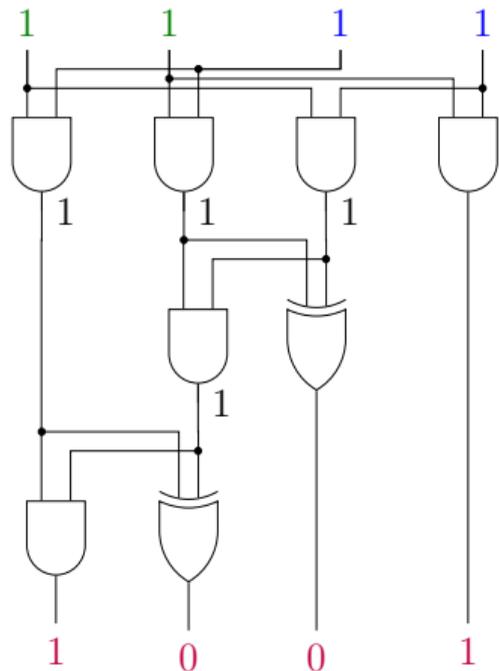
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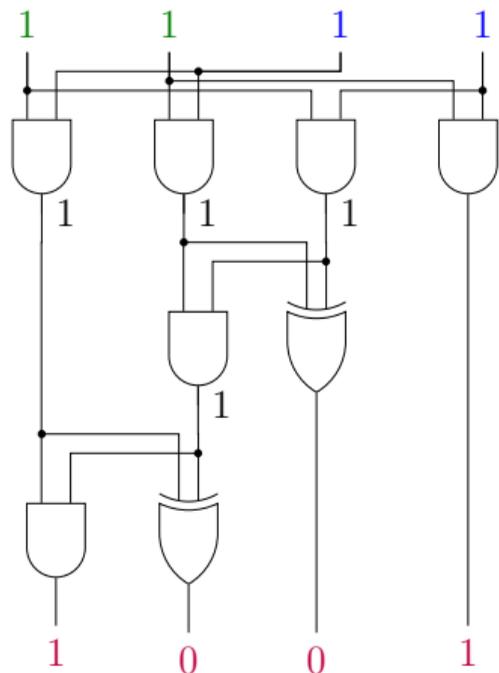
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Is the circuit correct?

# Multiplier circuit

$$\begin{array}{r} 11 \cdot 11 \\ \hline \phantom{11}11 \\ \phantom{11}110 \\ \hline 1001 \end{array}$$





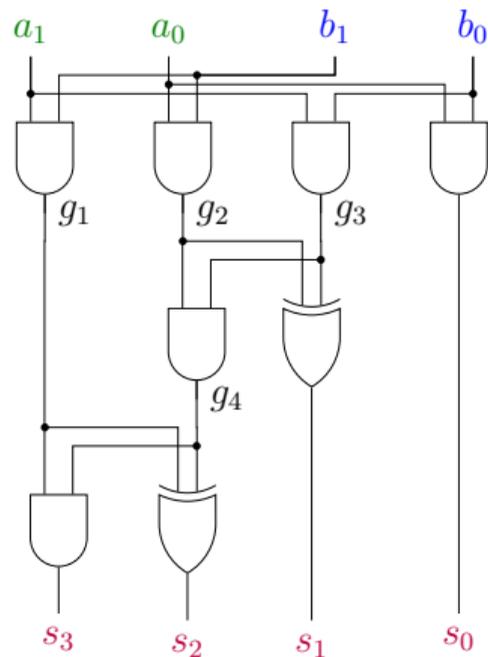
Is the circuit really correct?

# Multiplier Circuits

**Given:** Gate-level multiplier for fixed bit-width.

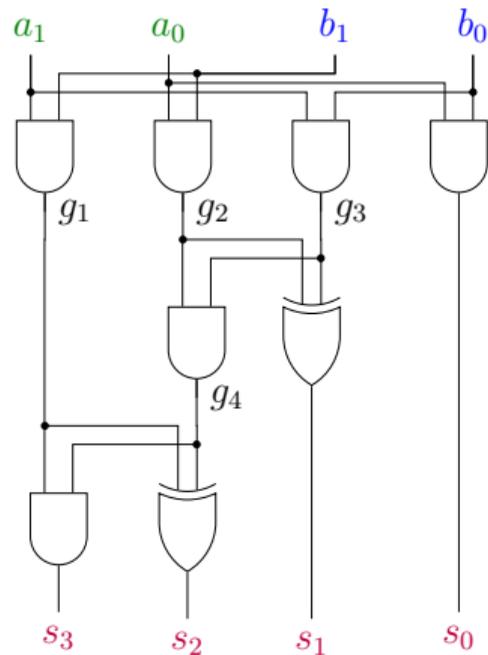
**Question:** For all possible  $a_i, b_i \in \mathbb{B}$  :

$$(2a_1 + a_0) * (2b_1 + b_0) = 8s_3 + 4s_2 + 2s_1 + s_0?$$



# Simulation

$a_1 a_0$	$\cdot$	$b_1 b_0$
00	$\cdot$	00
00	$\cdot$	01
00	$\cdot$	10
00	$\cdot$	11
01	$\cdot$	00
01	$\cdot$	01
01	$\cdot$	10
01	$\cdot$	11
10	$\cdot$	00
10	$\cdot$	01
10	$\cdot$	10
10	$\cdot$	11
11	$\cdot$	00
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11	$\cdot$	10
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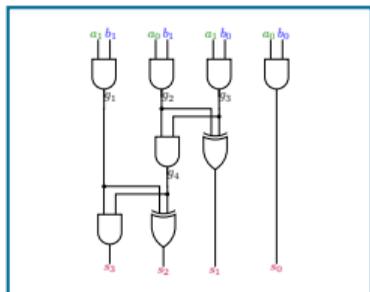


# Simulation

Bit-width	Cases	
2	16	
3	64	
4	256	
5	1 024	
6	4 096	
7	16 384	
8	65 536	
:	:	
:	:	
32	18 446 744 073 709 551 616	quintillion
:	:	
:	:	
64	340 282 366 920 938 463 463 374 607 431 768 211 456	undecillion

# Formal Verification

## System



## Specification

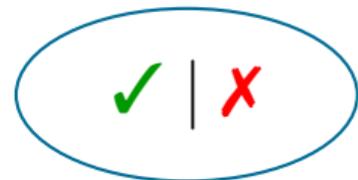
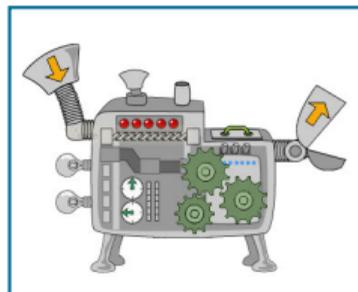
For all  $a_i, b_i \in \mathbb{B}$  :

$$(2a_1 + a_0) * (2b_1 + b_0) =$$
$$8s_3 + 4s_2 + 2s_1 + s_0?$$

## Mathematical Model

$$B = \{$$
$$x - a_0 * b_0,$$
$$y - a_1 * b_1,$$
$$s_0 - x * y,$$
$$\dots$$
$$\}$$

## Automated Decision Process



# Formal Verification Techniques

## Satisfiability Checking (SAT)

- SAT 2016 Competition

[Biere SATComp'16]

- Exponential run-time of solvers

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- First technique to detect Pentium bug

[ChenBryant DAC'95]

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[TemelSlobodovaHunt CAV'20]
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## Algebraic Approach

- Seminal work: [LvKallaEnescu TCAD'13, CiesielskiYuBrownLiuRossi DAC'15]  
[SayedGroßeKühneSoekenDrechsler DATE'16]
- Polynomial encoding
- Works for non-trivial multiplier designs

# Algebraic Approach

## Multipliers

- Finite Field Arithmetic

[LvKallaEnescu TCAD'13,  
SuYasinYuCiesielski ISCAS'18]

- Integer Arithmetic

[CiesielskiYuBrownLiuRossi DAC'15,  
SayedGroßeKühneSoekenDrechsler DATE'16,  
RitircBiereKauers FMCAD'17,  
MahzoonGroßeDrechsler ICCAD'18]

- Floating Point Arithmetic

[SayedGroßeSoekenDrechsler FMCAD'16]

## Dividers

- Division by a fixed constant

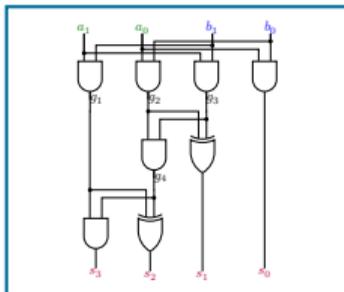
[YasinSuPillementCiesielski ISVLSI'19]

- General Divider Circuits

[SchollKonrad DAC'20,  
SchollKonradMahzoonGroßeDrechsler DATE'21]

# Basic Idea of Algebraic Approach

## Multiplier



## Polynomials

$$B = \left\{ \begin{array}{l} x - a_0 * b_0, \\ y - a_1 * b_1, \\ s_0 - x * y, \\ \dots \end{array} \right\}$$



## Specification

$$\sum_{i=0}^{2n-1} 2^i s_i - \left( \sum_{i=0}^{n-1} 2^i a_i \right) \left( \sum_{i=0}^{n-1} 2^i b_i \right)$$

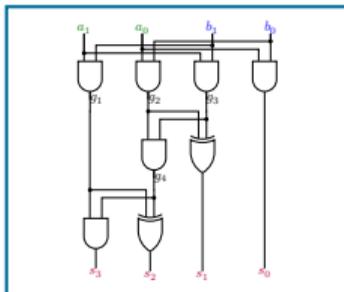


## Implication

$$\begin{array}{l} = 0 \quad \checkmark \\ \neq 0 \quad \times \end{array}$$

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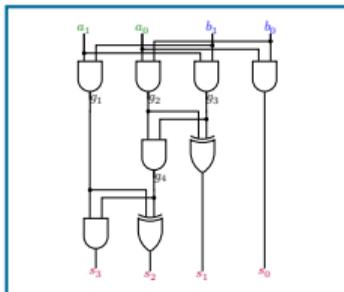


## Roots

$= 0$  ✓  
 $\neq 0$  ✗

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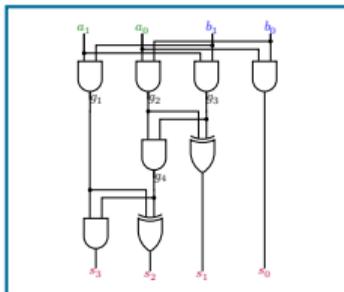


## Ideal Membership

$$\begin{array}{l} = 0 \quad \checkmark \\ \neq 0 \quad \times \end{array}$$

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$$\begin{array}{l} = 0 \quad \checkmark \\ \neq 0 \quad \times \end{array}$$

# Multiplier Specification

Unsigned Integers:

$$0 = \sum_{i=0}^{2n-1} 2^i s_i - \left( \sum_{i=0}^{n-1} 2^i a_i \right) \left( \sum_{i=0}^{n-1} 2^i b_i \right) \in \mathbb{Z}[X]$$

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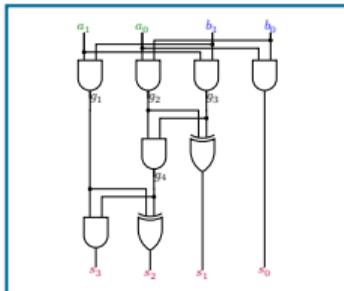
$$\sum_{i=0}^{2n-1} 2^i s_i - \left( \sum_{i=0}^{n-1} 2^i a_i \right) \left( \sum_{i=0}^{n-1} 2^i b_i \right) \in \mathbb{Z}[X]$$

**Signed Integers:**

$$-2^{2n-1} s_{2n-1} + \sum_{i=0}^{2n-2} 2^i s_i - \left( -2^{n-1} a_{n-1} + \sum_{i=0}^{n-2} 2^i a_i \right) \left( -2^{n-1} b_{n-1} + \sum_{i=0}^{n-2} 2^i b_i \right) \in \mathbb{Z}[X]$$

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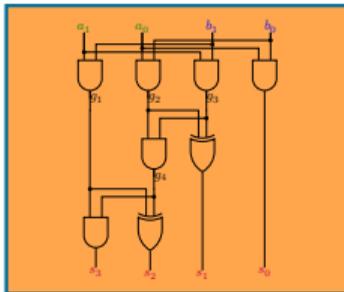
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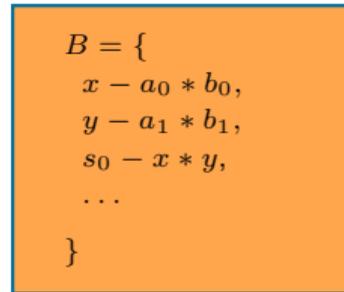
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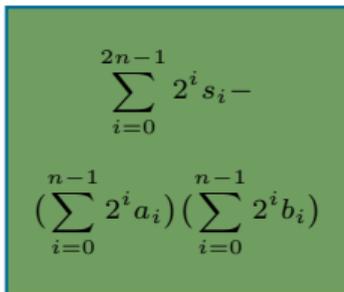
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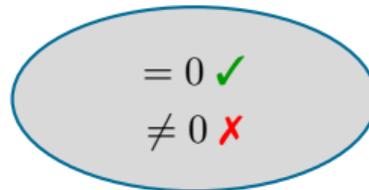
## Polynomials



## Specification



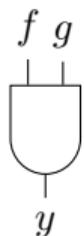
## Ideal Membership



# From Circuits to Polynomials

**AND-Gate**

$$f \wedge g = y$$



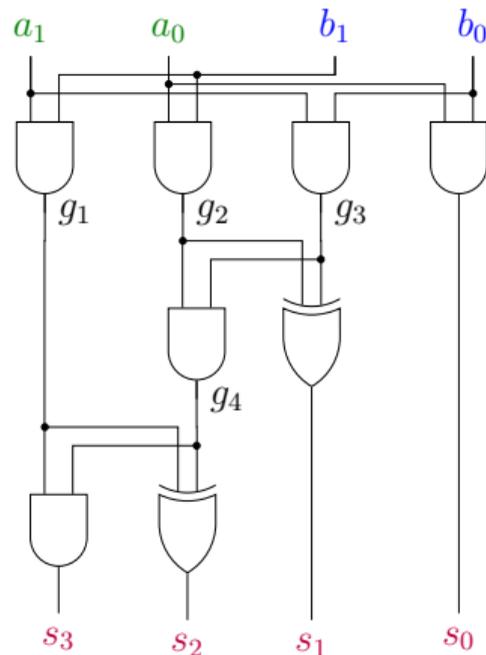
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$$f \oplus g = y$$



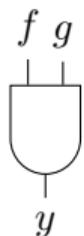
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**AND-Gate**

$$f \wedge g = y$$



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$$-y + fg$$

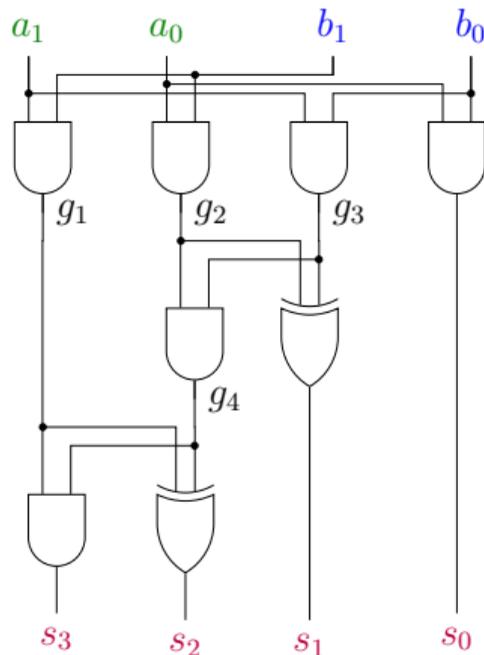
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1	1	0

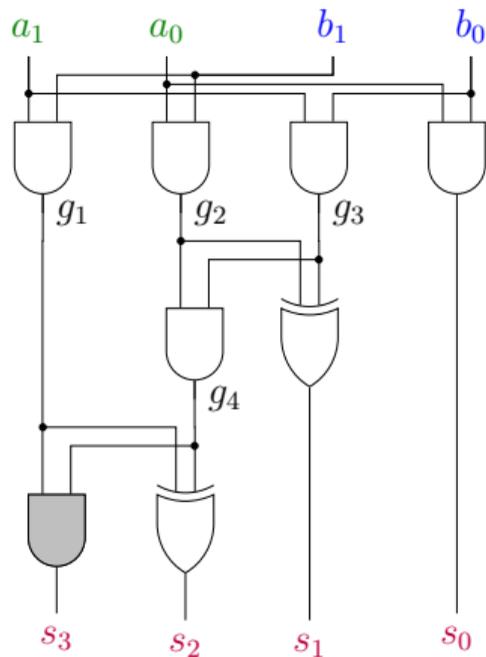
$$-y + f + g - 2fg$$



# From Circuits to Polynomials

Gate polynomials  $G(C)$ .

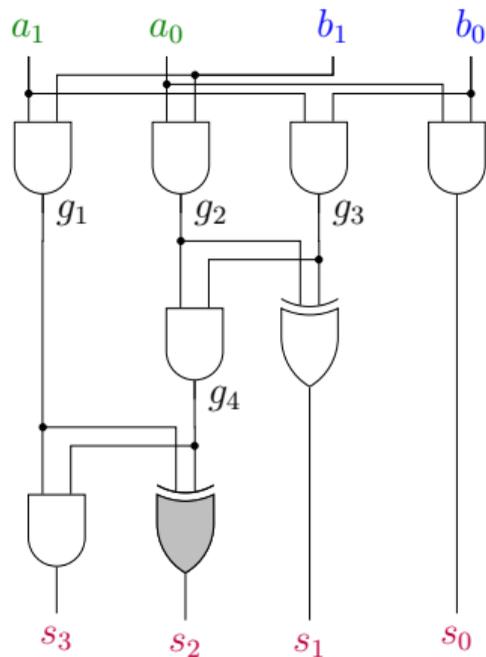
$$s_3 = g_1 \wedge g_4 \quad - s_3 + g_4 g_1,$$



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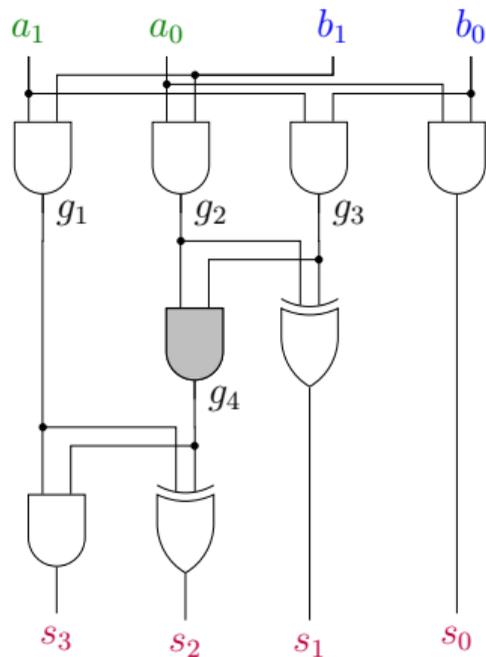
$$\begin{aligned} s_3 &= g_1 \wedge g_4 & -s_3 + g_4 g_1, \\ s_2 &= g_1 \oplus g_4 & -s_2 - 2g_4 g_1 + g_4 + g_1, \end{aligned}$$



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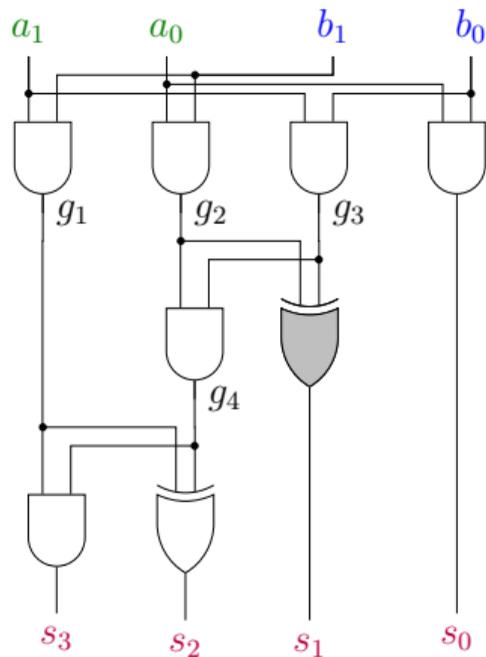
$$\begin{array}{ll} s_3 = g_1 \wedge g_4 & - s_3 + g_4 g_1, \\ s_2 = g_1 \oplus g_4 & - s_2 - 2g_4 g_1 + g_4 + g_1, \\ g_4 = g_2 \wedge g_3 & - g_4 + g_2 g_3, \end{array}$$



# From Circuits to Polynomials

Gate polynomials  $G(C)$ .

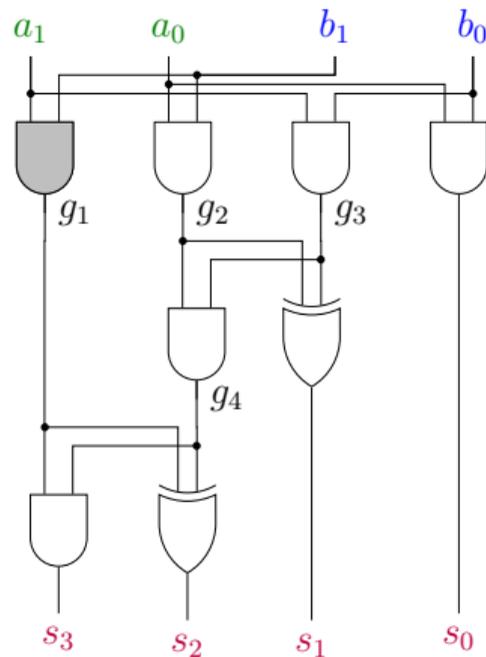
$$\begin{array}{ll} s_3 = g_1 \wedge g_4 & - s_3 + g_4 g_1, \\ s_2 = g_1 \oplus g_4 & - s_2 - 2g_4 g_1 + g_4 + g_1, \\ g_4 = g_2 \wedge g_3 & - g_4 + g_2 g_3, \\ s_1 = g_2 \oplus g_3 & - s_1 - 2g_2 g_3 + g_2 + g_3, \end{array}$$



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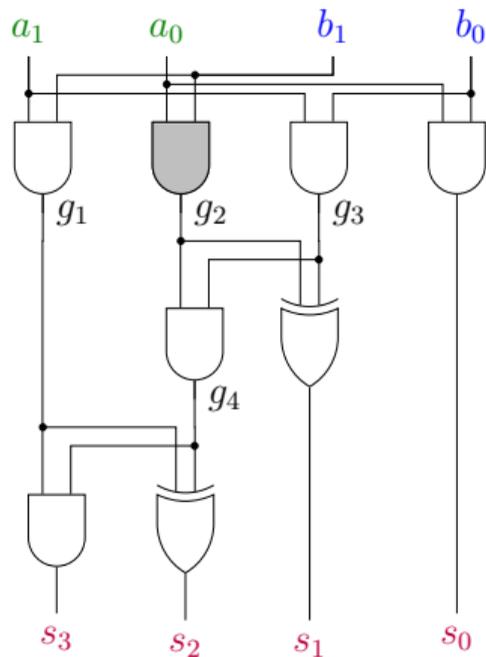
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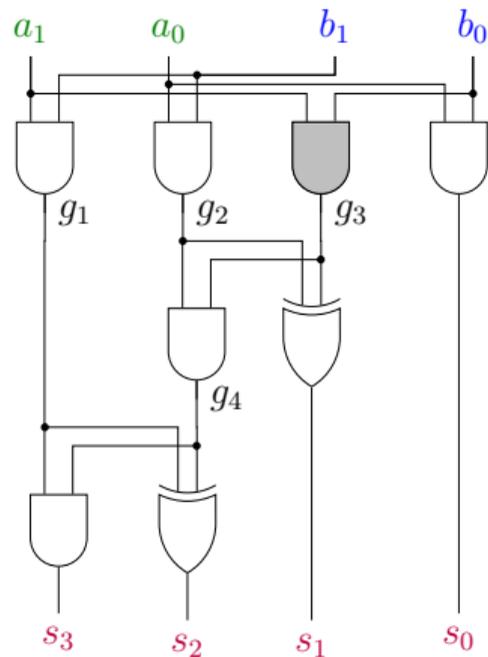
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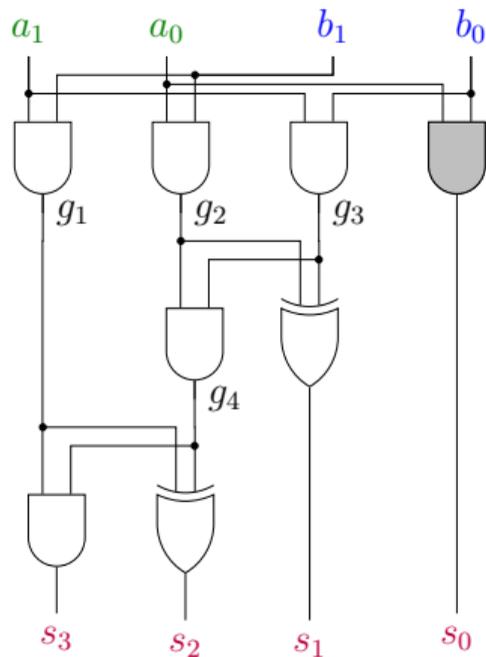
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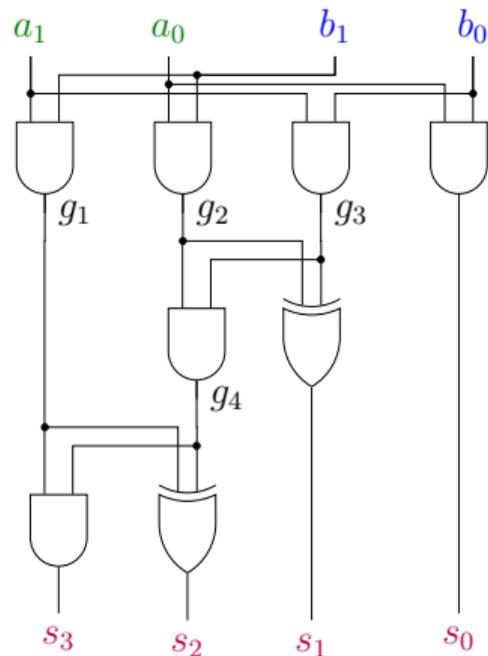
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Boolean value constraints  $B(C)$ .

$$\begin{array}{ll} a_1, a_0 \in \mathbb{B} & a_1(1 - a_1), a_0(1 - a_0), \\ b_1, b_0 \in \mathbb{B} & b_1(1 - b_1), b_0(1 - b_0) \end{array}$$



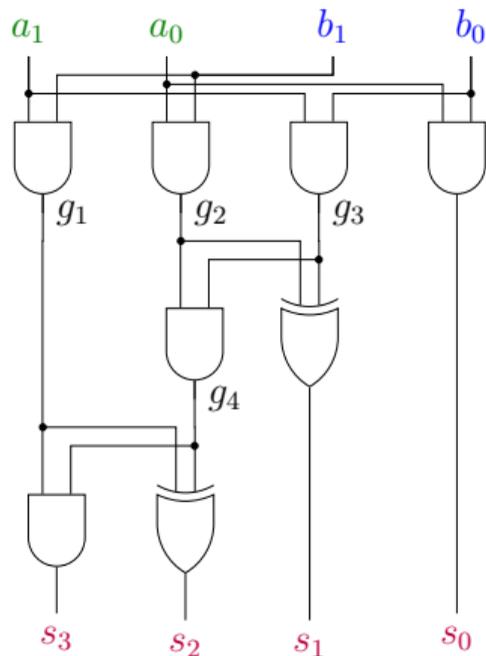
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Boolean value constraints  $B(C)$ .

$$\begin{array}{ll} a_1, a_0 \in \mathbb{B} & -a_1^2 + a_1, -a_0^2 + a_0, \\ b_1, b_0 \in \mathbb{B} & -b_1^2 + b_1, -b_0^2 + b_0 \end{array}$$



# Ideals Associated to Circuits

[RitircBiereKauers FMCAD'17, KaufmannBiereKauers FMSSD'20]

More circuit relations:

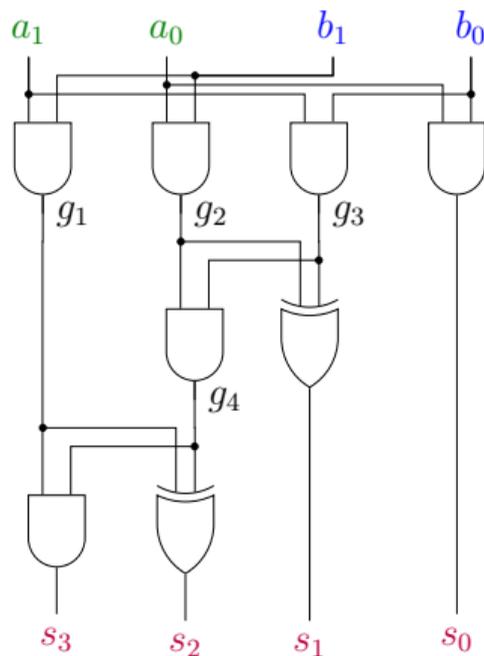
- $-s_0 + a_0b_0$  AND-gate
- $-a_1^2 + a_1$   $a_1$  Boolean
- $-g_2^2 + g_2$   $g_2$  Boolean
- $s_1g_4$  XOR-AND constraint
- ...

## Polynomial Circuit Constraints.

A polynomial  $p \in \mathbb{Z}[X]$  is a polynomial circuit constraint (PCC) if for all

$$(a_0, \dots, a_{n-1}, b_0, \dots, b_{n-1}) \in \{0, 1\}^{2n}$$

and resulting values  $g_1, \dots, g_k, s_0, \dots, s_{2n-1}$  implied by the gates of the circuit  $C$  the substitution of these values into  $p$  gives zero.



# Ideals Associated to Circuits

[RitircBiereKauers FMCAD'17, KaufmannBiereKauers FMSSD'20]

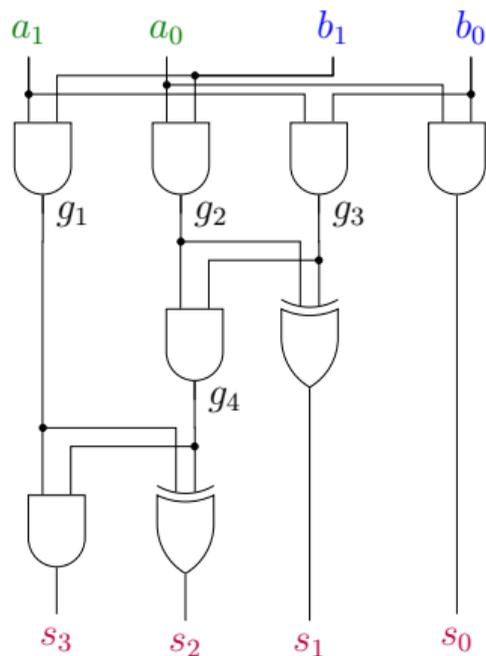
- The set of all PCCs for  $C$  is denoted by  $I(C)$ .
- $I(C)$  contains all relations of the circuit  $C$ .
- $I(C)$  is an ideal.

**Ideal.** A subset  $I \subseteq R[X]$  is called an ideal if

$$\forall p, q \in I : p+q \in I \quad \text{and} \quad \forall p \in R[X] \forall q \in I : pq \in I.$$

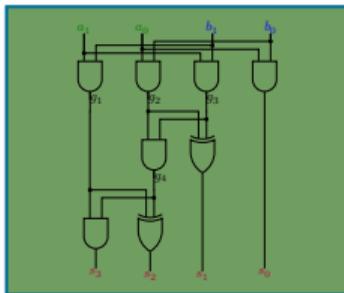
**Multiplier.** A circuit  $C$  is called a multiplier if

$$\sum_{i=0}^{2n-1} 2^i s_i - \left( \sum_{i=0}^{n-1} 2^i a_i \right) \left( \sum_{i=0}^{n-1} 2^i b_i \right) \in I(C).$$



# Basic Idea of Algebraic Approach

## Multiplier



## Polynomials

$$B = \left\{ \begin{array}{l} x - a_0 * b_0, \\ y - a_1 * b_1, \\ s_0 - x * y, \\ \dots \end{array} \right\}$$



## Specification

$$\sum_{i=0}^{2n-1} 2^i s_i - \left( \sum_{i=0}^{n-1} 2^i a_i \right) \left( \sum_{i=0}^{n-1} 2^i b_i \right)$$



## Ideal Membership

$$\begin{array}{l} = 0 \quad \checkmark \\ \neq 0 \quad \times \end{array}$$

## Ideal Membership Problem

**Basis.** A set  $G = \{g_1, \dots, g_m\} \subseteq R[X]$  is called a **basis** of an ideal  $I$  if

$$I = \{h_1g_1 + \dots + h_mg_m \mid h_1, \dots, h_m \in R[X]\} = \langle G \rangle$$

Given an arbitrary basis  $G$  of  $I$  it is not obvious how to decide ideal membership.

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**Gröbner basis.** [Buchberger'65]

- Offers unique decision procedure for ideal membership problem.
- Every ideal has a finite Gröbner basis.
- Given an arbitrary basis of an ideal, we are able to compute a Gröbner basis.

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- Offers unique decision procedure for ideal membership problem.
- Every ideal has a finite Gröbner basis.
- Given an arbitrary basis of an ideal, we are able to compute a Gröbner basis.
- Computing a Gröbner basis and deciding ideal membership is EXPSPACE-complete.[Mayr STACS'89]

# Ideal Membership Problem

[RitircBiereKauers FMCAD'17]

- We can deduce some elements of  $I(C)$ :
  - Gate polynomials  $G(C)$
  - Boolean value constraints  $B(C)$
- Let  $J(C) = \langle G(C) \cup B(C) \rangle$ .
- Lexicographic term order: Reverse topological  
Output variable of a gate is greater than input variables [LvKallaEnescu TCAD'13].

## Theorem

$G(C) \cup B(C)$  is a Gröbner basis for  $J(C)$ .

Proof idea: Application of Buchberger's Product criterion.

# Soundness and Completeness

[RitircBiereKauers FMCAD'17]

## Theorem

*For all acyclic circuits  $C$ , we have  $J(C) = I(C)$ .*

- $J(C) \subseteq I(C)$ : soundness
- $I(C) \subseteq J(C)$ : completeness

# Non-Incremental Checking Algorithm

## Verification Algorithm

Reduce specification  $\sum_{i=0}^{2n-1} 2^i s_i - \left(\sum_{i=0}^{n-1} 2^i a_i\right) \left(\sum_{i=0}^{n-1} 2^i b_i\right)$  by elements of  $G(C) \cup B(C)$

until no further reduction is possible, then  $C$  is a multiplier iff remainder is zero.

# Verification

$$G(C) \cup B(C) = \{$$

$$-s_3 + g_1g_4,$$

$$-s_2 - 2g_1g_4 + g_4 + g_1,$$

$$-g_4 + g_2g_3,$$

$$-s_1 - 2g_2g_3 + g_3 + g_2,$$

$$-g_1 + a_1b_1,$$

$$-g_2 + a_0b_1,$$

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$$8s_3 + 4s_2 + 2s_1 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0$$

$$8g_1g_4 + 4s_2 + 2s_1 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0$$

$$4g_4 + 4g_1 + 2s_1 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0$$

$$4g_2g_3 + 4g_1 + 2s_1 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0$$

$$4g_1 + 2g_3 + 2g_2 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0$$

$$2g_3 + 2g_2 + s_0 - 2a_1b_0 - 2a_0b_1 - a_0b_0$$

$$2g_3 + s_0 - 2a_1b_0 - a_0b_0$$

$$s_0 - a_0b_0$$

$$0$$

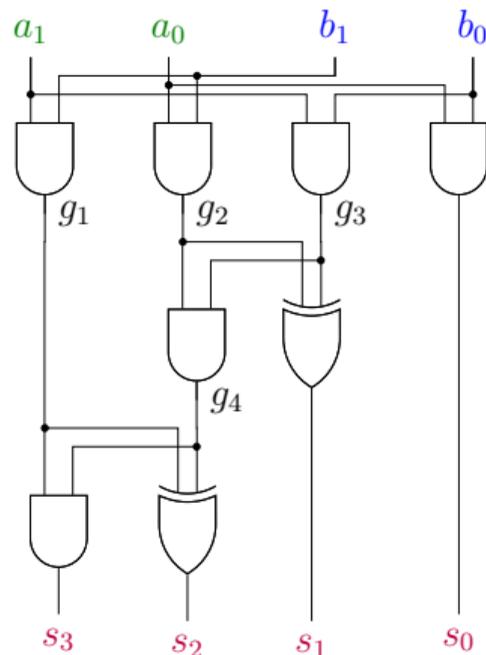
# Faulty multiplier

## Gate polynomials $G(C)$ .

$$\begin{array}{ll} s_3 = g_1 \wedge g_4 & -s_3 + g_4 g_1, \\ s_2 = g_1 \oplus g_4 & -s_2 - 2g_4 g_1 + g_4 + g_1, \\ g_4 = g_2 \wedge g_3 & -g_4 + g_2 g_3, \\ s_1 = g_2 \oplus g_3 & -s_1 - 2g_2 g_3 + g_2 + g_3, \\ g_1 = a_1 \wedge b_1 & -g_1 + a_1 b_1, \\ g_2 = a_0 \wedge b_1 & -g_2 + a_0 b_1, \\ g_3 = a_1 \wedge b_0 & -g_3 + a_1 b_0, \\ s_0 = a_0 \wedge b_0 & -s_0 + a_0 b_0 \end{array}$$

## Boolean value constraints $B(C)$ .

$$\begin{array}{ll} a_1, a_0 \in \mathbb{B} & a_1(1 - a_1), a_0(1 - a_0), \\ b_1, b_0 \in \mathbb{B} & b_1(1 - b_1), b_0(1 - b_0) \end{array}$$



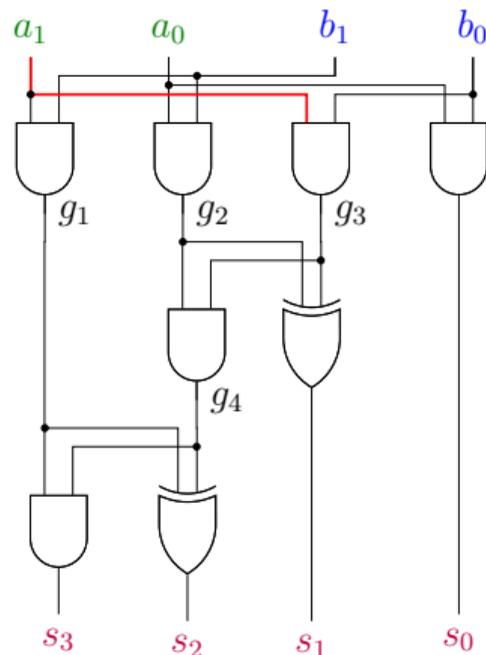
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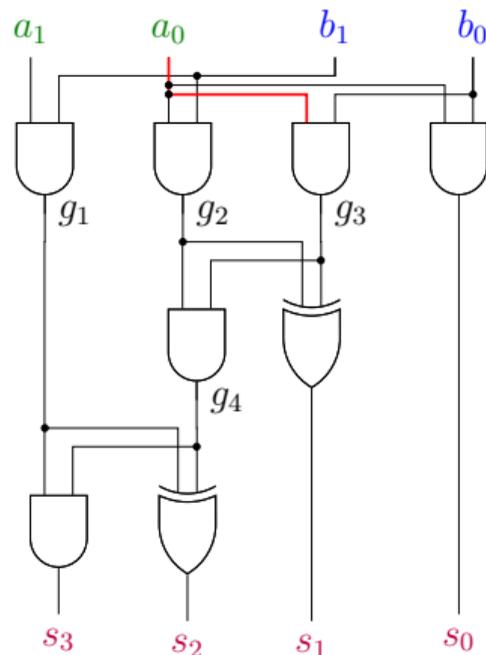
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## Verification of a faulty multiplier

$$G(C) \cup B(C) = \{$$

$$-s_3 + g_1g_4,$$

$$-s_2 - 2g_1g_4 + g_4 + g_1,$$

$$-g_4 + g_2g_3,$$

$$-s_1 - 2g_2g_3 + g_3 + g_2,$$

$$-g_1 + a_1b_1,$$

$$-g_2 + a_0b_1,$$

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$$-s_0 + a_0b_0,$$

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$$2g_3 + s_0 - 2a_1b_0 - a_0b_0$$

$$s_0 - 2a_1b_0 + a_0b_0$$

$$-2a_1b_0 + 2a_0b_0$$

## Counter Example

Remainder:  $-2a_1b_0 + 2a_0b_0 \neq 0$

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$$a_1 = 0, \quad a_0 = 1$$

$$b_1 = 0, \quad b_0 = 1$$

$$01 \cdot 01 = 0001$$

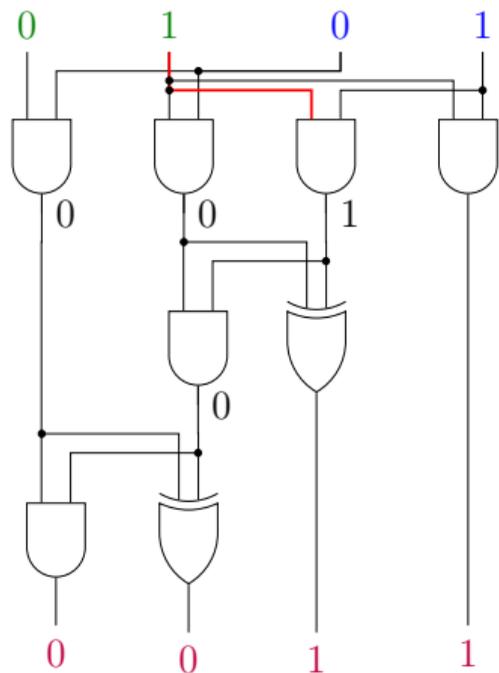
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# Error Correction using Algebra

Uses the remainder polynomial to compute rectification functions that nullify errors.

- **Single-fix** [FarahmandiMishra ICCD'17, MahzoonGroßeDrechsler ISVLSI'18]
- **Multi-fix** [RaoOndricekKallaEnescu VLSI-SoC'21, SabbaghAlizadeh ETS'21]

Limited application, as they rely on existence of remainder polynomial.

# Non-Incremental Checking Algorithm

## Verification Algorithm

Reduce specification  $\sum_{i=0}^{2n-1} 2^i s_i - \left(\sum_{i=0}^{n-1} 2^i a_i\right) \left(\sum_{i=0}^{n-1} 2^i b_i\right)$  by elements of  $G(C) \cup B(C)$

until no further reduction is possible, then  $C$  is a multiplier iff remainder is zero.

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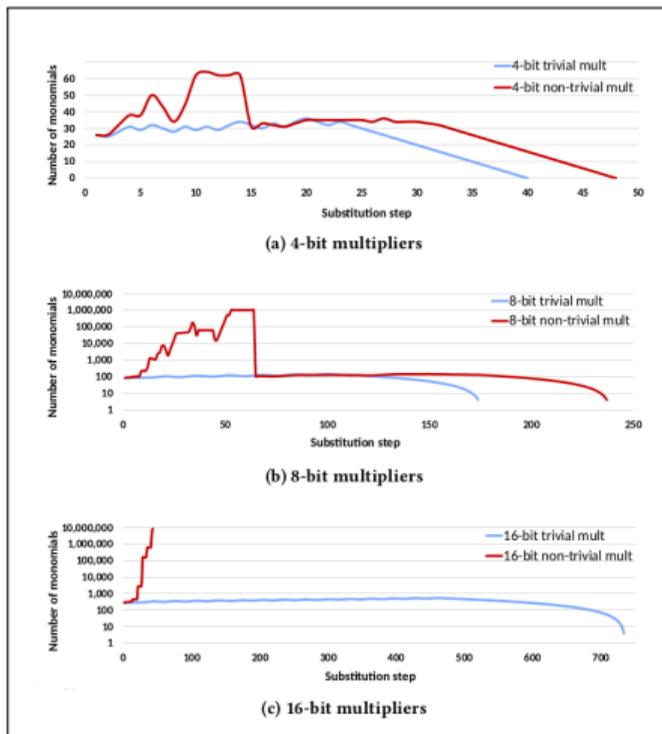
until no further reduction is possible, then  $C$  is a multiplier iff remainder is zero.

## Computational Problems

- The number of monomials in the intermediate results increases drastically.
- 8-bit multiplier cannot be verified within 20 minutes.

# Non-Incremental Checking Algorithm

[MahzoonGroßeDrechsler ICCAD'18]



# Strategies

## 1. Preprocessing

- Variable Elimination [MahzoonGroßeDrechsler DAC'19, RitircBiereKauers DATE'18]

## 2. Reduction

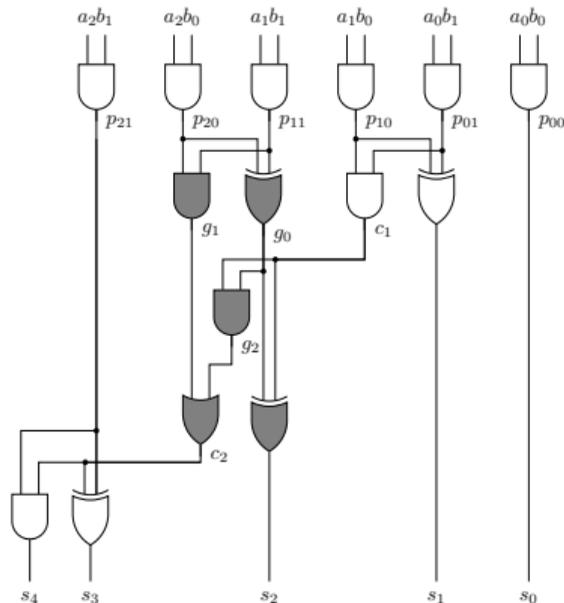
- Incremental Algorithm [RitircBiereKauers FMCAD'17]
- Dynamic Reduction Order [MahzoonGroßeSchollDrechsler DATE'20]

## 3. Tricky: OR Gates in final stage adder

- Include SAT or BDDs [KaufmannBiereKauers FMCAD'19, DrechslerMahzoon ISEEIE'22]
- Dual variables [KaufmannBeameBiereNordström DATE'22]

# Preprocessing - Variable Elimination

[RitircBiereKauers DATE'18, MahzoonGroßeDrechsler DAC'19]



## Full adder

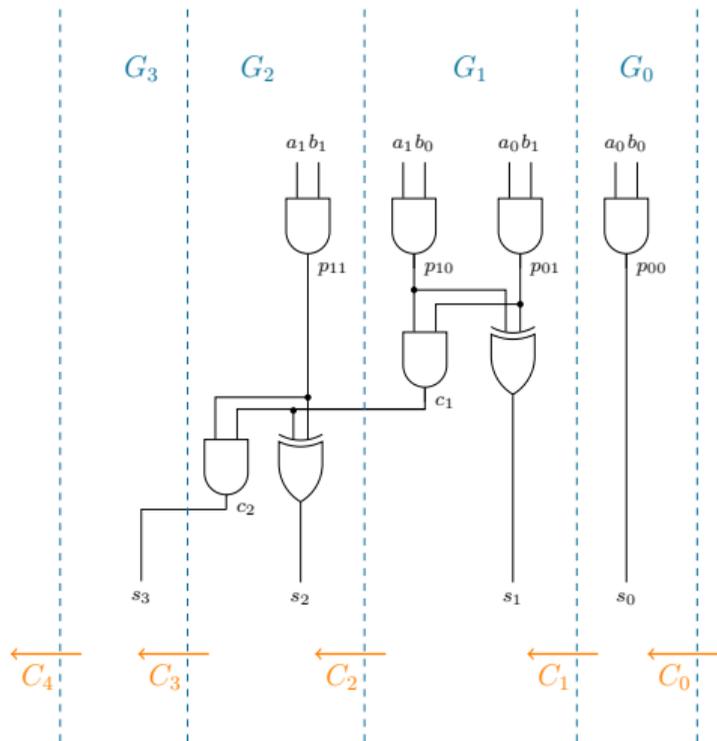
$$\left. \begin{aligned} & -c_2 + g_2 + g_1 - g_2g_1, \\ & -s_2 + g_0 + c_1 - 2g_0c_1, \\ & -g_2 + g_0c_1, \\ & -g_1 + p_{20}p_{11}, \\ & -g_0 + p_{20} + p_{11} - 2p_{20}p_{11} \end{aligned} \right\} -2c_2 - s_2 + p_{20} + p_{11} + c_1$$

**Theorem** ([RitircBiereKauers DATE'18])

*Local elimination of variables preserves Gröbner basis.*

# Incremental Verification

[RitircBiereKauers FMCAD'17]



$$\text{Let } P_k = \sum_{k=i+j} a_i b_j.$$

## Column-Wise Checking Algorithm

Input: Circuit  $C$  with sliced Gröbner bases  $G_i$

Output: Determine whether  $C$  is a multiplier

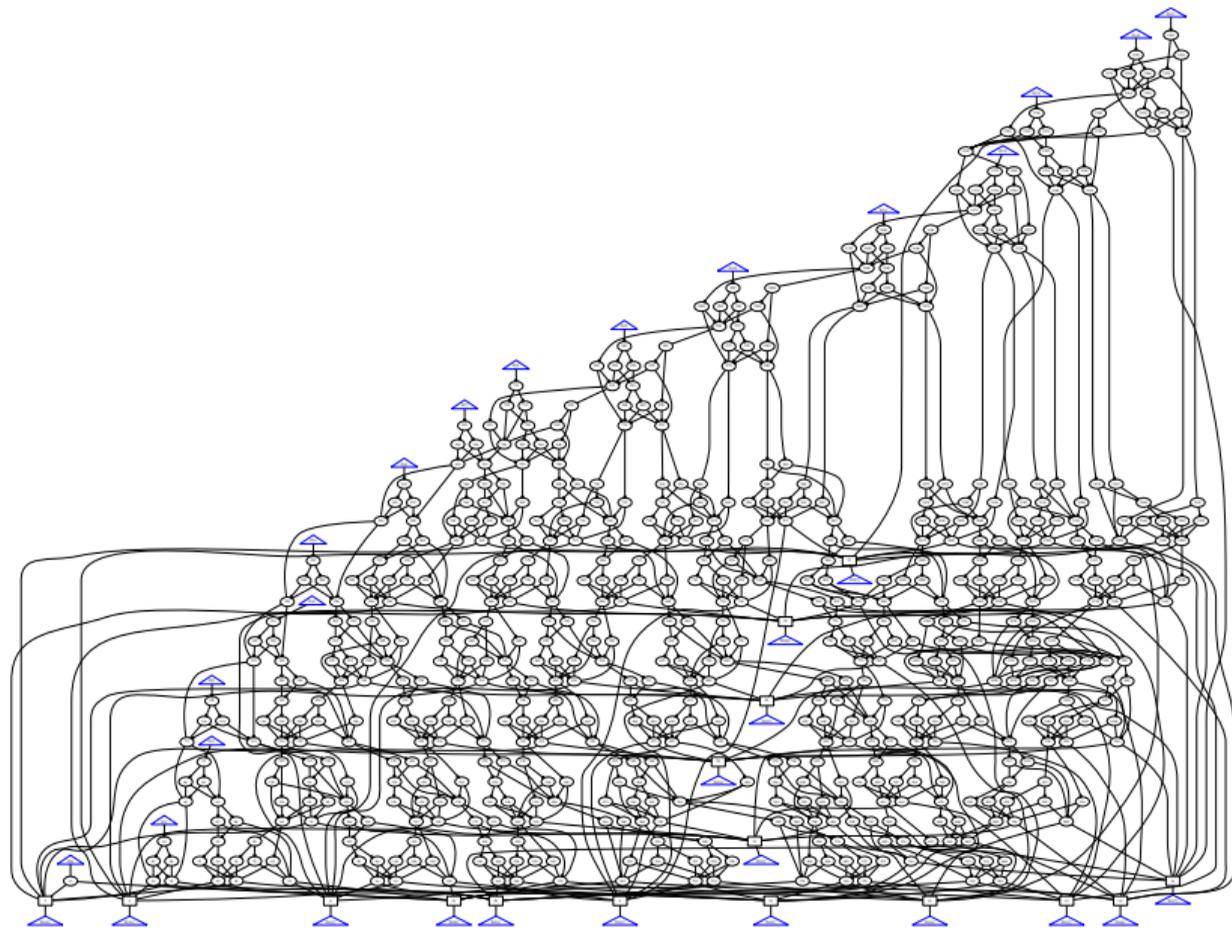
$$C_{2n} \leftarrow 0$$

**for**  $i \leftarrow 2n - 1$  **to** 0

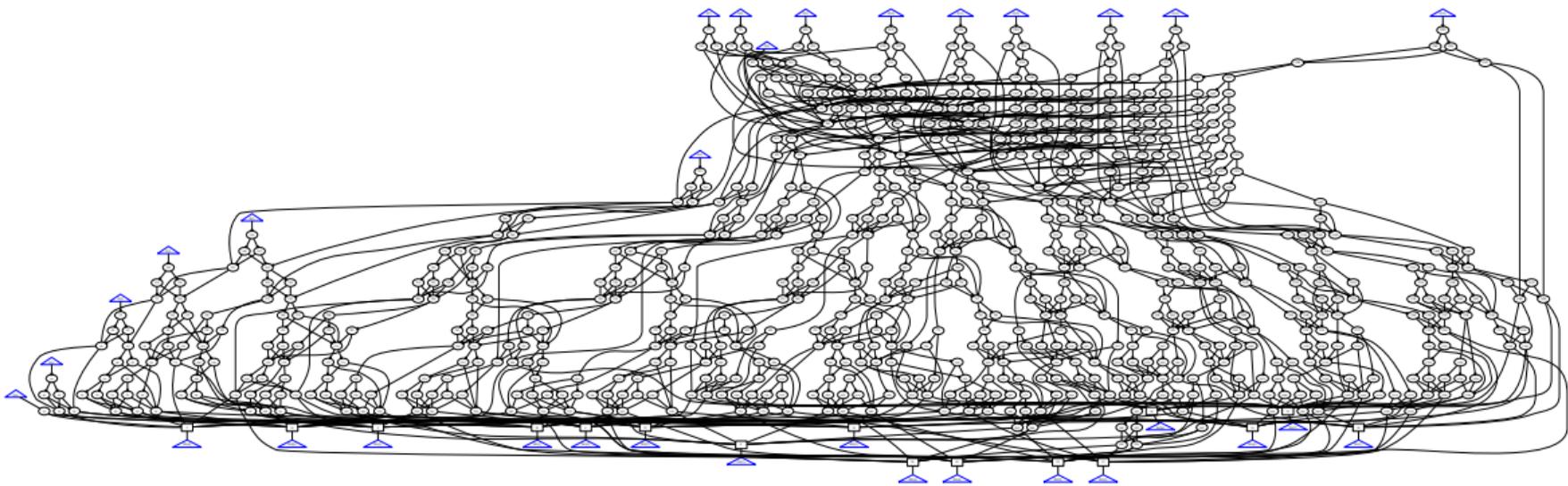
$$C_i \leftarrow \text{Remainder}(2C_{i+1} + s_i - P_i, G_i)$$

**return**  $C_0 = 0$

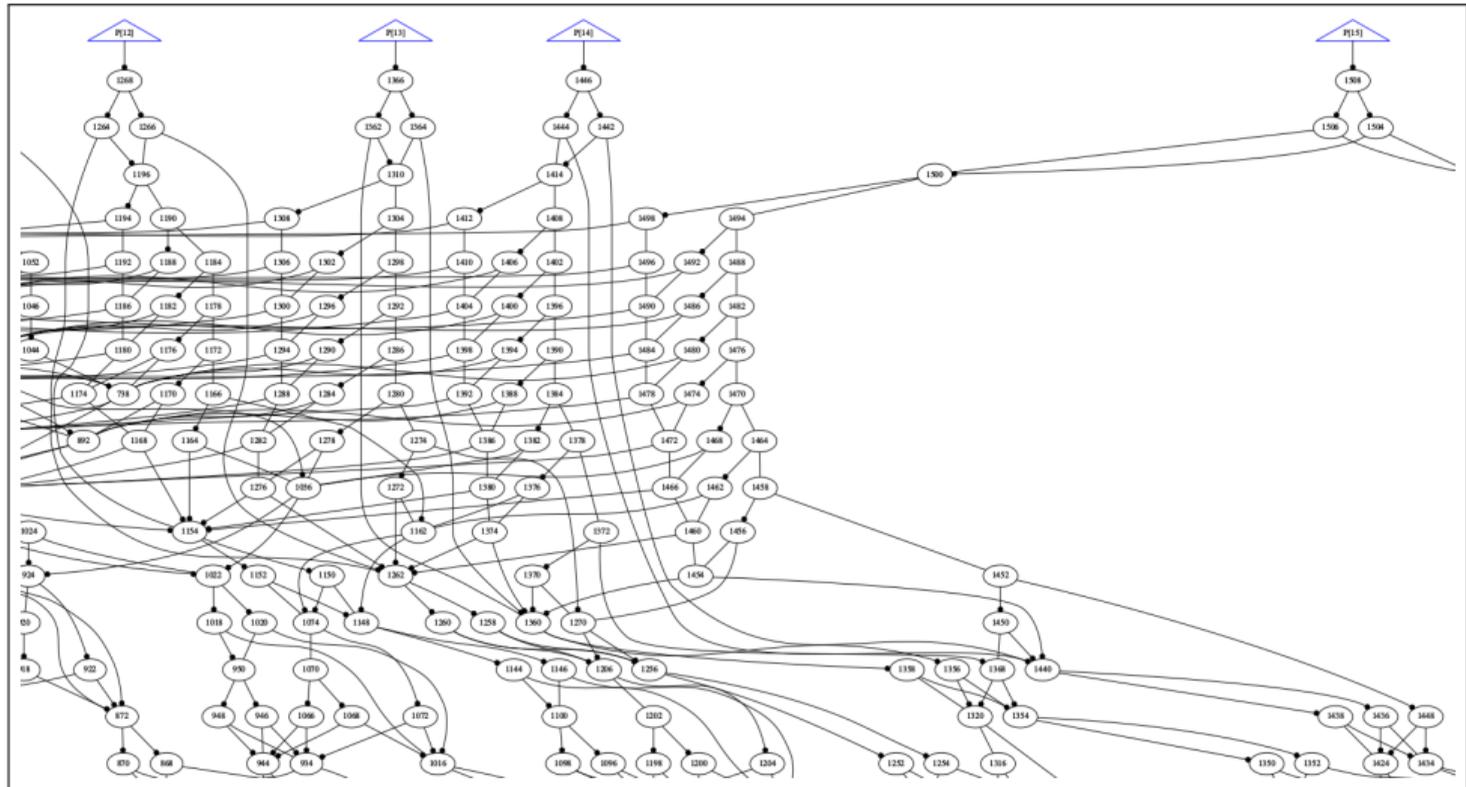
# Simple



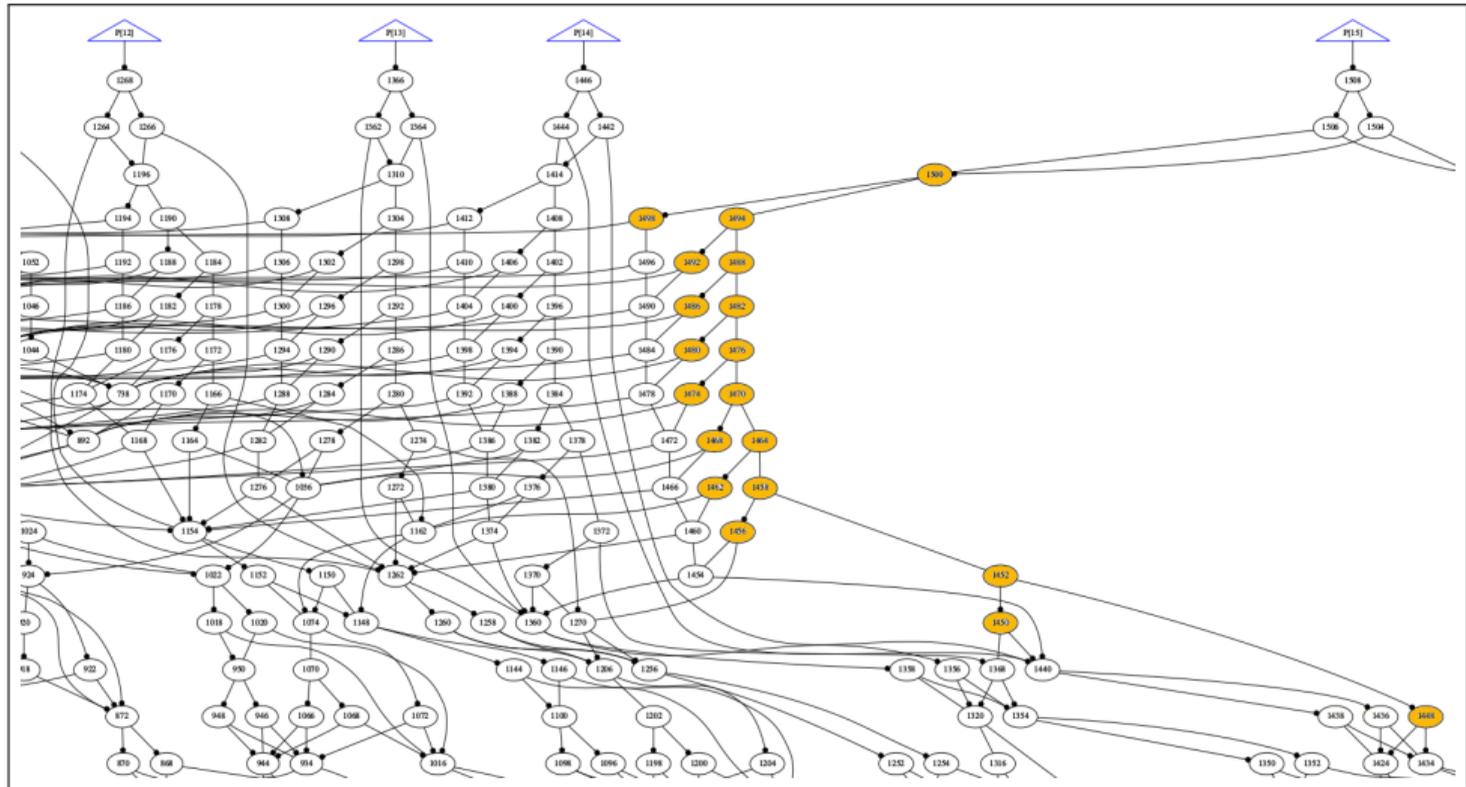
# Hard



# Hard

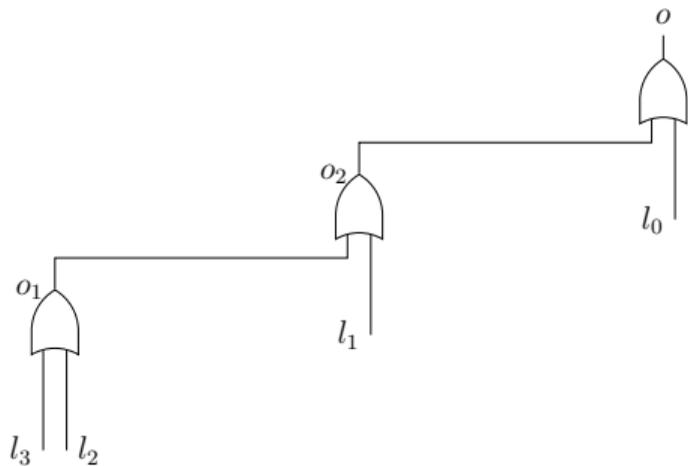


# Hard



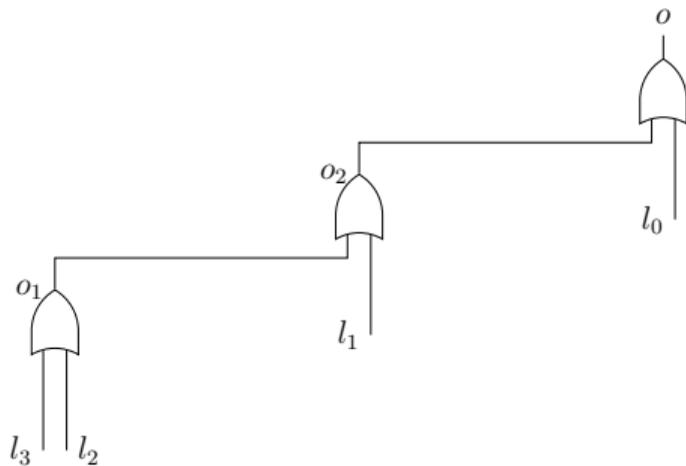
# OR Gates

$$\begin{aligned}o &= o_2 \vee x_0 & -o + o_2 + l_0 - o_2l_0, \\o_2 &= o_1 \vee l_1 & -o_2 + o_1 + l_1 - o_1l_1, \\o_1 &= l_3 \vee l_2 & -o_1 + l_3 + l_2 - l_3l_2\end{aligned}$$



# OR Gates

$$\begin{aligned}o &= o_2 \vee l_0 & -o + o_2 + l_0 - o_2l_0, \\o_2 &= o_1 \vee l_1 & -o_2 + o_1 + l_1 - o_1l_1, \\o_1 &= l_3 \vee l_2 & -o_1 + l_3 + l_2 - l_3l_2\end{aligned}$$



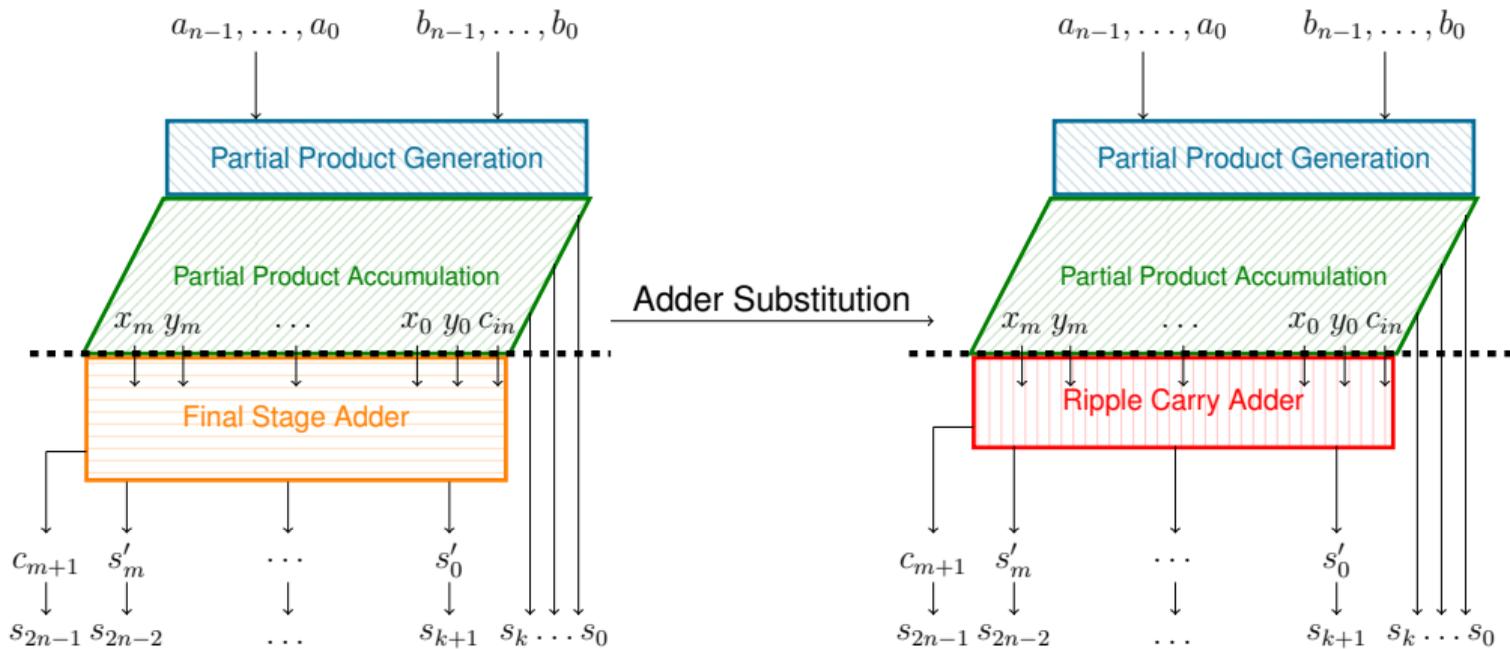
$$o = l_0 + l_1 - l_0l_1 + l_2 - l_0l_2 - l_1l_2 + l_0l_1l_2 + l_3 - l_0l_3 - l_1l_3 + l_0l_1l_3 - l_2l_3 + l_0l_2l_3 + l_1l_2l_3 - l_0l_1l_2l_3$$

$15 = 2^4 - 1$  monomials

$n$  OR Gates  $\rightarrow 2^{n+1} - 1$  monomials

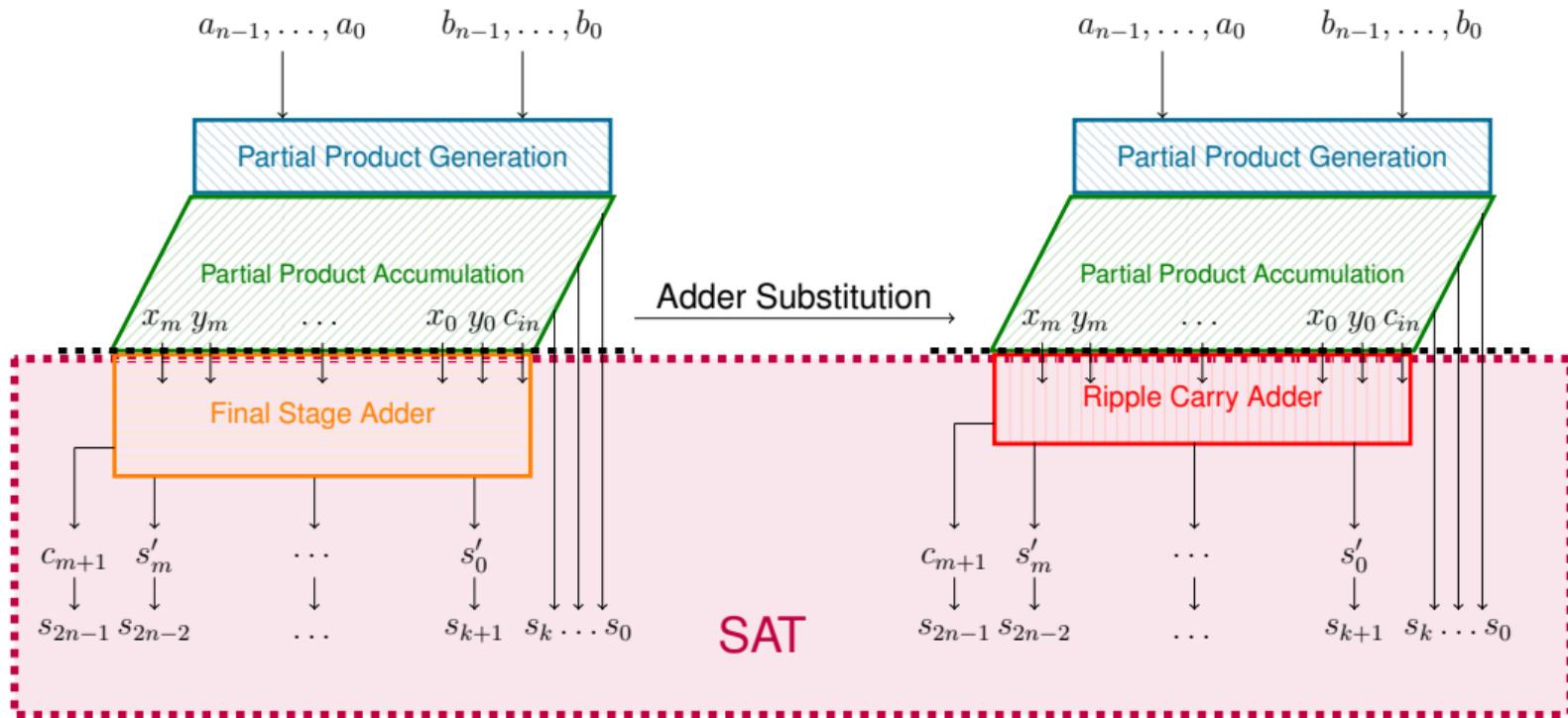
# SAT & Computer Algebra

[KaufmannBiereKauers FMCAD'19]



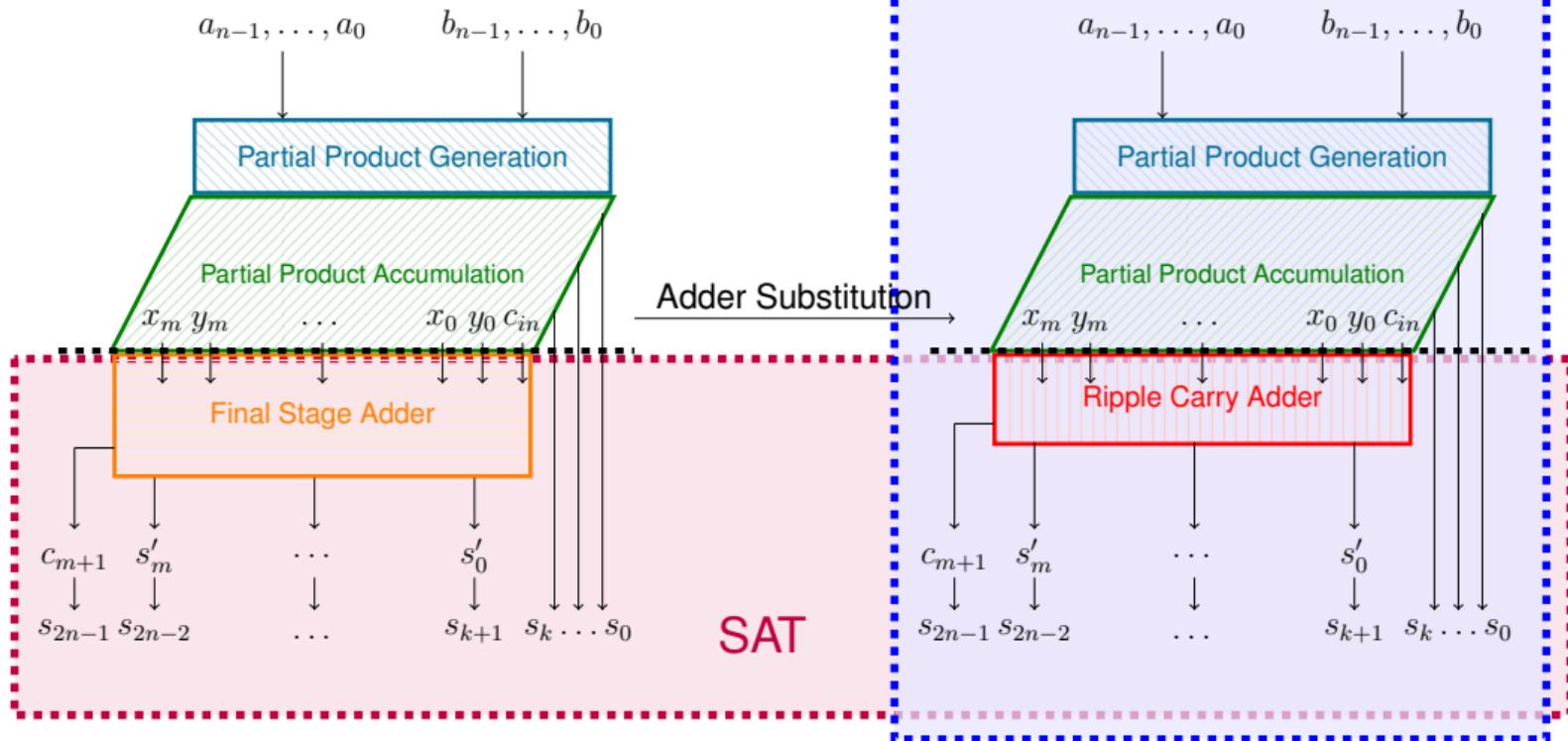
# SAT & Computer Algebra

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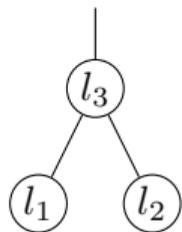
# SAT & Computer Algebra

[KaufmannBiereKauers FMCAD'19]

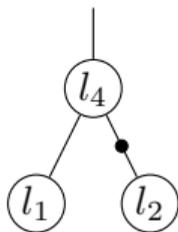


# Dual Variables

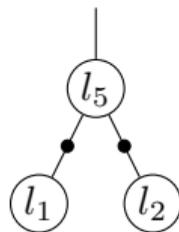
Provide a shorthand notation for inverters.



$$l_3 = l_1 \wedge l_2$$
$$-l_3 + l_1 l_2$$



$$l_4 = l_1 \wedge \neg l_2$$
$$-l_4 - l_1 l_2 + l_1$$



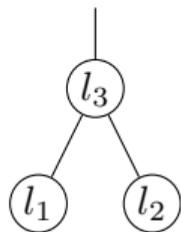
$$l_5 = \neg l_1 \wedge \neg l_2$$
$$-l_5 + l_1 l_2 - l_1 - l_2 + 1$$

# Dual Variables

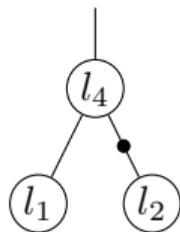
Provide a shorthand notation for inverters.

## Dual variables.

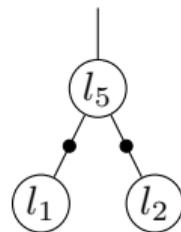
Whenever two variables  $l_i, f_i \in \{0, 1\}$  fulfill the relation  $f_i = 1 - l_i$ , we have  $f_i = \text{dual}(l_i)$ .



$$l_3 = l_1 \wedge l_2$$
$$-l_3 + l_1 l_2$$
$$-l_3 + l_1 l_2$$



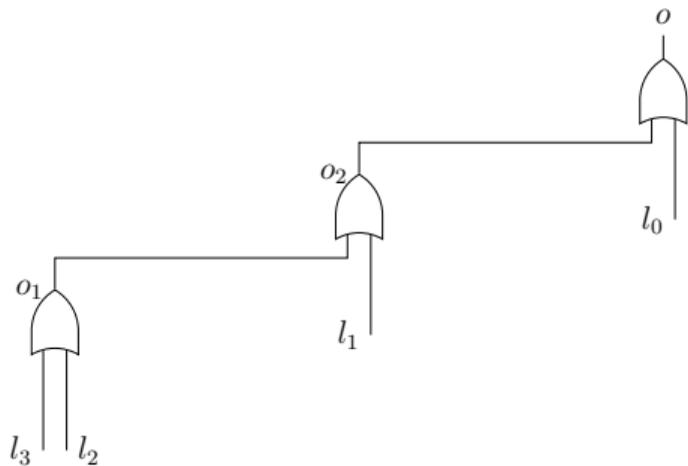
$$l_4 = l_1 \wedge \neg l_2$$
$$-l_4 - l_1 l_2 + l_1$$
$$-l_4 + l_1 f_2$$



$$l_5 = \neg l_1 \wedge \neg l_2$$
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# OR Gates

$$\begin{aligned}o &= o_2 \vee x_0 & -o + o_2 + l_0 - o_2 l_0, \\o_2 &= o_1 \vee l_1 & -o_2 + o_1 + l_1 - o_1 l_1, \\o_1 &= l_3 \vee l_2 & -o_1 + l_3 + l_2 - l_3 l_2\end{aligned}$$

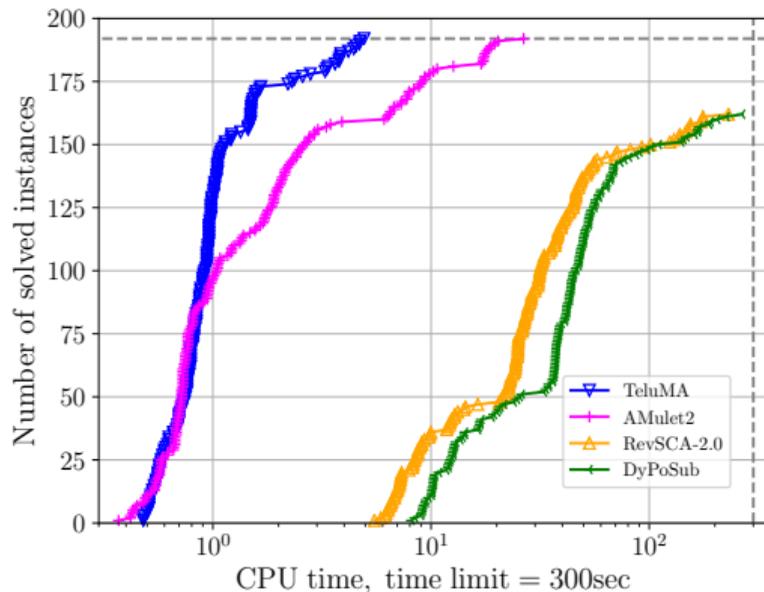


$$o = l_0 + l_1 - l_0 l_1 + l_2 - l_0 l_2 - l_1 l_2 + l_0 l_1 l_2 + l_3 - l_0 l_3 - l_1 l_3 + l_0 l_1 l_3 - l_2 l_3 + l_0 l_2 l_3 + l_1 l_2 l_3 - l_0 l_1 l_2 l_3$$

$$o = 1 - f_0 f_1 f_2 f_3$$

# Evaluation - Multiplier Verification

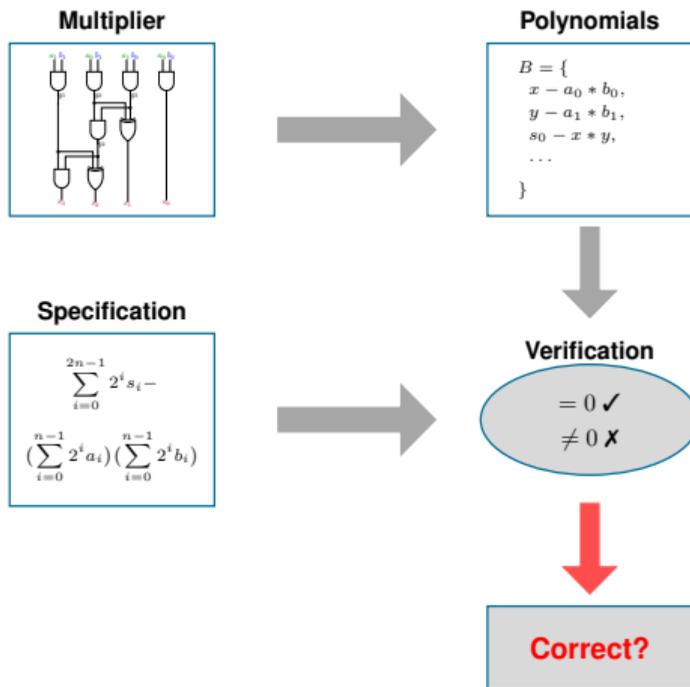
Verification of 192 unsigned 64-bit multipliers



- **TeluMA** [KaufmannBeameBiereNordström DATE'22]  
variable elimination - incremental reduction - dual var.
- **AMulet2** [KaufmannBiere TACAS'21]  
variable elimination - incremental reduction - SAT
- **RevSCA-2.0** [MahzoonGroßeDrechsler DAC'19]  
variable elimination
- **DyPoSub** [MahzoonGroßeSchollDrechsler DATE'20]  
variable elimination - dynamic reduction

Is the circuit really really correct?

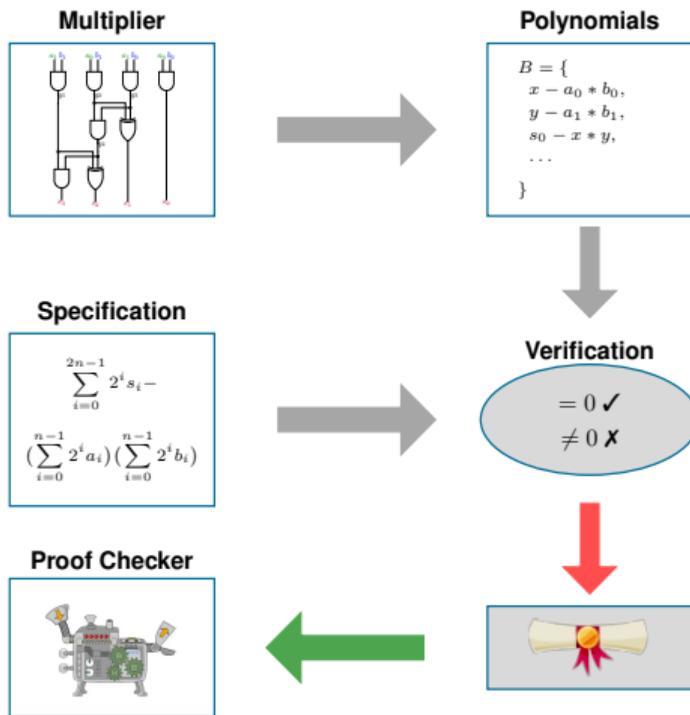
# Proofs



## Problem:

- Can we trust our own implementation?
- Is the verification process correct?

# Proofs



## Problem:

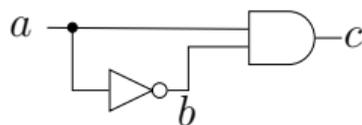
- Can we trust our own implementation?
- Is the verification process correct?

## Solution:

Validate result of verification process.

- Generate machine-checkable proofs.
- Check by independent proof checkers.

# Practical Algebraic Calculus



$$G(C) = \{-b + 1 - a, -c + ab\}$$

$$B(C) = \{-a^2 + a\}$$

$$\text{Spec} = c$$

[RitircBiereKauers SC2'18]

```
* : -b+1-a,      a,      -a*b+a-a^2;
* : -a^2+a,      -1,      a^2-a;
+ : -a*b+a-a^2,  a^2-a,   -a*b;
+ : -a*b,        -c+a*b,   -c;
* : -c,          -1,      c;
```

[KaufmannFleuryBiere FMCAD'20]

```
3 * 1,  a,  -a*b;
1 d;
4 + 3,  2,  -c;
5 * 4,  -1,  c;
```

[KaufmannBiereKauers FMCAD'19]

```
* : -b+1-a,  a,      -a*b;
+ : -a*b,    -c+a*b,  -c;
* : -c,      -1,      c;
```

[KaufmannFleuryBiereKauers FMSSD'21]

```
3 % 1*(-a) + 2*(-1), c;
```

Is the circuit really really really correct?

# PASTÈQUE

[KaufmannFleuryBiere FMCAD'20]

**Theorem Prover** Isabelle/HOL



**Refinement Approach**, relying on Isabelle's Refinement Framework

- abstract specification on ideals: specification in ideal
- final step: executable checker

**Isabelle's Archive of Formal Proofs** 8000 lines of code

# Conclusion

- **Is the circuit correct?**

Yes, because we have tested some cases.

- **Is the circuit *really* correct?**

Yes, because we applied algebraic reasoning.

- **Is the circuit *really really* correct?**

Yes, because we generated and checked a proof certificate.

- **Is the circuit *really really really* correct?**

Yes, because we used a verified proof checker.

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